WHAT IS CLAIMED IS:

1. A read and write assist and restore circuit for a memory device, comprising:

a first device being responsive to a potential on a bit line such that the potential on the bit line activates the first device; and

a second device driven by the first device such that when the first device is activated, a change in the bit line potential is reinforced with positive feedback by the second device during a wordline active period to enable write-back of data lost as a result of threshold voltage fluctuations in memory cell transistors coupled to the bit line.

2. The circuit as recited in claim 1, further comprising a select circuit, which selectively enables the circuit.

3. The circuit as recited in claim 1, further comprising a virtual ground, which includes a higher

potential than a global ground to assist in write operations.

4. The circuit as recited in claim 3, wherein the virtual ground is pinned to a voltage above ground potential during write operations and standby.

5. The circuit as recited in claim 3, wherein the virtual ground is connected to the global ground through a transistor device to collapse a difference in potential between the global ground and the virtual ground during read access mode.

6. The circuit as recited in claim 1, wherein the first device includes a transistor and a gate of the transistor is coupled to the bit line.

7. The circuit as recited in claim 1, wherein the second device includes a transistor and a gate of the transistor of the second device is coupled to a supply

voltage through the first device.

8. The circuit as recited in claim 1, wherein the second device assists the bit line by discharging current from the bit line when the second device is activated.

9. The circuit as recited in claim 1, wherein the first device is self-timing such that the first device is only active when the first device senses changes in bit line voltage.

10. The circuit as recited in claim 1, wherein the first and second devices include body biased transistors.

11. A read and write assist and restore circuit for a memory device, comprising:

a sensing device responsive to a potential on a bit line such that the potential on the bit line activates the sensing device;

a driver device driven by the sensing device such that

when the sensing device is activated, a change in the bit line potential is reinforced with positive feedback by the second device during a wordline active period to enable write-back of data lost as a result of threshold voltage fluctuations in memory cell transistors coupled to the bit line; and

a virtual ground, which provides a higher potential than a global ground to the memory cell transistors to assist in write operations and during standby.

12. The circuit as recited in claim 11, further comprising a select circuit, which selectively enables the circuit.

13. The circuit as recited in claim 11, wherein the virtual ground is pinned to a voltage higher than ground potential during write operations and standby.

14. The circuit as recited in claim 11, wherein the virtual ground is connected to the global ground through a

transistor device to collapse a difference in potential between the global ground and the virtual ground during read access mode.

15. The circuit as recited in claim 11, wherein the sensing device includes a transistor and a gate of the transistor is coupled to the bit line.

16. The circuit as recited in claim 11, wherein the driver device includes a transistor and a gate of the transistor of the driver device is coupled to a supply voltage through the sensing device.

17. The circuit as recited in claim 11, wherein the driver device assists a selected memory cell by discharging current from the bit line when the driver device is activated.

18. The circuit as recited in claim 11, wherein the sensing device is self-timing such that the sensing device

is only active when the sensing device senses sufficient voltage change in the bit line.

19. The circuit as recited in claim 11, wherein the sensing and driver devices include body biased transistors.